Amendments to the Specification:

Please amend the specification as follows:

Please replace the paragraph starting at page 1, after the title of the application and before "BACKGROUND OF THE INVENTION" with the following rewritten paragraph:

~~This application is a Continuation-in-Part of Application No. 07/992,653, filed December 18, 1992.~~ This application is a continuation of application Serial No. 09/722,474, filed November 28, 2000 (the entire contents of which are incorporated herein by reference), which is a continuation of application Serial No. 09/283,583, filed April 1, 1999 now U.S. Patent No. 6,172,911, which is a continuation of application Serial No. 09/100,330, filed June 19, 1998 now U.S. Patent No. 5,909,399, which is a continuation of 08/826,820, filed April 8, 1997 now U.S. Patent No. 5,793,696, which is a continuation of application Serial No. 08/784,927, filed January 16, 1997 now U.S. Patent No. 5,724,300, which is a continuation of application Serial No. 08/576,564, filed December 21, 1995 now U.S. Patent No. 5,615,165, which is a continuation of application Serial No. 08/326,281, filed October 20, 1994 now U.S. Patent No. 5,546,351, which is a continuation-in-part of application Serial No. 07/992,653, filed December 18, 1992 now U.S. Patent No. 5,361,227.

Please replace the paragraph starting at page 3, line 23, with the following rewritten paragraph:

However, it is difficult for a conventional data write method to make the range of the threshold value of a memory cell written with data ~~"1"~~ 0 enter such an allowable range, because the conventional data write method writes data by using the same condition for all memory cells while using a fixed write potential and write time for all memory cells. More specifically, the characteristic of each memory cell changes with variation of manufacturing processes, sometimes resulting in a memory cell easy to be written and at other times

resulting in a memory cell difficult to be written. Considering such a write characteristic difference, there has been proposed a data write method which controls the data write time for verifying the written data, in order to set the threshold value of each memory cell within a desired range.

Please replace the paragraph starting at page 11, line 34, with the following rewritten paragraph:

Fig. 93 is a cross sectional view taken along line ~~B-B'~~ 93-93 of Fig. 92.

Please replace the paragraph starting at page 11, line 36, with the following rewritten paragraph:

Fig. 94 is a cross sectional view taken along line ~~C-C'~~ 94-94 of Fig. 92.

Please replace the paragraph starting at page 13, line 1, with the following rewritten paragraph:

Figs. 2(a) and 2(b) are plan views and a NAND of a memory cell array, and an equivalent circuit diagram. Figs 3(a) and 3(b) are cross sectional views taken along lines A-A' and B-B' of Fig 2(a). A memory cell array is formed within a p-type region 11 surrounded by an element isolation oxide film 12, the memory cell array having a plurality of memory cells or NAND cells. In the following, one NAND cell will be described. In this embodiment, one NAND cell is constituted by eight memory cells M1 to M8 connected in series. Each memory cell has a floating gate 14 (14_1, 14_2 ... 14_8) above a substrate 11 with a gate insulating film 13 being interposed therebetween. Above the floating gate 14, a control gate 16 (16_1, 16_2 ... 16_8) is formed with an interlayer insulating film 15 interposed therebetween. Each n-type diffusion layer 19 is shared by two adjacent memory cells, one as a source and the other as a drain. In this way, memory cells are connected in series.

Please replace the paragraph starting at page 58, line 15, with the following rewritten paragraph:

Figs. 70(a), (b) and (c) ~~and (b)~~ show another example of the rewrite setting transistors T11 and T12. The diagram indicated by Fig. 70(a) shows the transistors T11 and T12 described previously, and the diagram indicated by Fig. 70(b) shows another example of the transistors T11 and T12. By using a transistor having a threshold voltage near 0 V as the transistor T11, it is possible to set "H" level on the bit line near to Vcc in the verify mode. It is more effective to apply a raised potential to the gate of the transistor T12. Namely, the potential drop (threshold drop) relative to the power supply voltage Vcc becomes small, providing a large margin in the read operation.

Please replace the paragraph starting at page 60, line 13, with the following rewritten paragraph:

In order to solve this problem, as shown if Figure 79 the source of the verify setting circuit is connected via a transistor T_A to the source of each memory cell. The gate of the transistor T_A is applied with a signal PROVERI which takes "H" level during the program verify operation. In this way, the source of the verify setting circuit is set to the level of the source of each memory cell. Therefore, the source potential change of each memory cell can be reflected upon.

Please replace the paragraph starting at page 71, line 21, with the following rewritten paragraph:

Fig. 91 is a plan view of a pattern, Fig. 93 is a cross sectional view taken along line ~~B-B'~~ 93-93 of Fig. 92, and Fig. 94 is a cross sectional view taken along line ~~C-C'~~ 94-94 of Fig. 92. In these figures, reference numeral 211 represents a floating gate (FG) made of a first

layer polysilicon. Reference numeral 212 represents a control gate (CG) made of a second layer polysilicon. The control gate 212 is used as the word line of a memory cell.